REMARKS

Claims 1 - 22 are pending in this application, of which claims 4, 5 and 17 - 20 have been withdrawn from consideration. By this Amendment, claims 1, 9, 14, 16 and 21 have been amended. No new claims have been added. It is respectfully submitted that this Amendment is fully responsive to the Office Action dated August 27, 2002.

Examiner Interview:

The courtesy extended by Examiner Chen during the December 19, 2002 personal interview is gratefully acknowledged. The substance of discussions during the interview are incorporated into the following remarks.

New Matter Rejection:

In item 2 of the outstanding Action, the Preliminary Amendment filed 2/25/02 is objected to under 35 U.S.C. §132 due to the Examiner's contention that the feature of "the wiring composed from different material from the local interconnection" added to both independent claims 1 and 21 is not supported by the specification as originally filed.

This objection is respectfully traversed.

It is respectfully submitted that this objection is now moot since such objected to language has been deleted from each of independent claims 1 and 21. More specifically, each of the independent claims 1 and 21 now call for forming a wiring electrically connecting to the other of the couple of impurity diffusion layers, the wiring composed from multi-layer films, the wiring having lower resistance than the local interconnection. According, withdrawal of this objection is respectfully submitted.

35 U.S.C. §112, First Paragraph, Rejection:

Claims 1 - 3, 6 - 16 and 21 - 22 stand rejected under 35 U.S.C. §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

This rejection is respectfully traversed.

As discussed above, the language "the wiring composed from different material from the local interconnection" has been deleted from each of the independent claims 1 and 21, thereby rendering this rejection moot. Accordingly, withdrawal of this rejection is respectfully solicited.

35 U.S.C. §112, Second Paragraph, Rejection:

Claims 9 and 14 - 16 stand rejected in item 5 under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

This rejection is respectfully traversed.

It is respectfully submitted that each of claims 9, 14 and 16 have been amended to overcome this rejection. Accordingly, withdrawal of this rejection is respectfully solicited.

As To The Merits

As to the merits of the case, while the Examiner has withdrawn his previous rejections based **Ochiai**, **Watanabe et al.**, **Zafar** and **Yamazaki et al.**, the Examiner now sets forth the following rejections:

(1) claims 1 - 3, 9, 11 - 16 and 21 - 22 stand rejected under 35 U.S.C. § 102(e) as being anticipated by **Mochizuki et al.** (of record); and

(2) claims 6 - 8 and 10 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over **Mochizuki et al.** in view of **Kawai et al.** (of record).

Each of these rejections are respectfully traversed.

Independent claims 1 and 21, as amended, now call for *forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view, the entire portion being with respect to a width and a length of the upper electrode, in a range which passes through the first opening and the second opening, by patterning the metal film.*

None of the applied references, singly or in combination, teach or fairly suggest the significant structural arrangements of the applicants' claim invention concerning forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view the entire portion being with respect to a width and a length of the upper electrode, in a range which passes through the first opening and the second opening, by patterning the metal film.

It is a purpose of the invention to prevent deterioration of polarization-characterization caused by a diffusion of hydrogen in the step of forming the third insulating film and the local interconnection by a CVD using a reduction reaction. Therefore, the local interconnection is formed on the capacitor as covering an entire section of the upper electrode of the capacitor, and the local interconnection becomes the layer for preventing the diffusion of the hydrogen.

As shown in Fig. 2B (appended sheet), in the present invention, a capacitor (slash part) is entirely covered by a local interconnection 9a in order to prevent that the capacitor from being exposed to the reduction atmosphere. That is, the local interconnection 9a covers the entire portion of the upper electrode 7 with respect to both a width and a length of the upper electrode 7.

Ordinarily, as shown in Fig. 4A (appended sheet), only a part of a capacitor (slash part) is covered by a local interconnection 30a, and it is not considered that the capacitor is exposed to the reduction atmosphere.

Meanwhile, the examiner points out that the feature of the present invention is disclosed in the section view of **Mochizuki**. But if a plan view is considered from the constitution of Fig. 19 of **Mochizuki**, the local interconnection is formed on a portion of the capacitor (a region surrounded by the thick line) as shown in Figs. 4A-I (appended sheet). In other words, the local interconnection 30a fails to cover the upper electrode 7 with respect to the width of the upper electrode 7.

That is, while an edge portion of a local interconnection in Figs. 17, 19, 20, 21 and 23 of **Mochizuki** maybe arranged above an edge portion of one side of a capacitor, however, in a plan view, as shown Fig. 8, since the local interconnection 22 is formed inside the upper electrode 19,

clearly, the local interconnection 22 does not cover an entire portion of the upper electrode 19 with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view. In other words, **Mochizuki** is absent any teaching or disclosure concerning the local interconnection 22 covering the upper electrode 19 with respect to the width of the upper electrode 19.

Accordingly, since hydrogen is the smallest element, the hydrogen is diffused to the capacitor via a second insulating film from an edge portion of the local interconnection. That is, diffusion to the capacitor of hydrogen used in the step of forming the third insulating film on the local interconnection can not be prevented in **Mochizuki** completely since, as shown in the plan view of Fig. 8 of **Mochizuki**, local interconnection 22 does not cover an entire portion of the upper electrode 19. More specifically, local interconnection 22 does not cover the entire width of the upper electrode 19.

In **Mochizuki**, since there is no technical idea which is to prevent that the capacitor is exposed to reduction atmosphere by covering an entire portion of the capacitor with only a local interconnection, it is unthinkable that the local interconnection is formed to cover the entire portion above the capacitor.

Once there is no above technical idea in **Mochizuki**, persons skilled in the art can not easily think the feature that the local interconnection is formed to cover the entire portion above the capacitor.

Accordingly, the feature of the present invention is not disclosed in **Mochizuki** and the present invention technical idea is not easily devised from **Mochizuki**.

Further, independent claims 1 and 21, as amended, now additionally call for *forming a wiring electrically connecting to the other of the couple of impurity diffusion layers, the wiring composed from multi-layer films, the wiring having lower resistance than the local interconnection.*

That is, in the present claimed invention, as amended, the impurity diffusion layer is formed by a couple of impurity diffusion layers, wherein the local interconnection is electrically connected to one of the couple of impurity diffusion layers, and the wiring is electrically connected to the other of the couple of impurity diffusion layers. Moreover, the wiring has lower resistance than the local interconnection. For example, since the wiring includes an Al film, it is clear that a resistance of the wiring is lower than a resistance of the local interconnection.

Thus, the local interconnection which connects to one of the couple of impurity diffusion layers and is formed to cover the capacitor can give priority to preventing capacitor degradation by

reduction gas. Further, the wiring which is connected to the other of the couple of impurity diffusion layers and whose resistance is lower than the local interconnection can give priority to a higher conductivity than a reduction prevention action.

For example, as described in Fig. 1G, the local interconnection 9a(TiN) is electrically connected to one 3d of the impurity diffusion layers (3s,3d), and the second wiring 13 (multiplayer including A1) is electrically connected to the other 3s of impurity diffusion layers (3s, 3d). Thus, as described in claims 2 and 3, in the case that a TiN layer as the local interconnection9a is applied, the TiN layer is superior as a reduction prevention layer than an Al layer (second wiring 13), and, since a fusing current of the TiN layer is higher than that of the Al layer, the TiN layer can be used with a thin thickness unlike the Al layer.

Thus, in the case of conduction between a short distance (local interconnection and the like), since a wiring resistance does not become a problem, the TiN local interconnection having a thin thickness can be used. In this matter, since the local interconnection having a thin thickness as a reduction prevention layer can be used, the step of planarization is not necessary and a low cost process is constructed.

In contrast, in **Mochizuki**, wiring (al layer 22/TiN layer 11' etc.) composed from the same material is respectively connected to a couple of impurity diffusion layers 33,34. Since priority is

given only to the high conductivity of wiring, diffusion of the reduction gas to the capacitor cannot be prevented completely. Moreover, since the step of planarization of the circumference of the capacitor is needed, the process becomes complicated.

As above explanation, features of amended claims 1 and 21 are completely different from the cited documents. That is, the cited documents do not describe that the wiring is composed from multi-layer films, the wiring having lower resistance than the local interconnection, wherein the local interconnection is a reduction preventing layer of the capacitor and the local interconnection is formed to cover the entire portion above the capacitor.

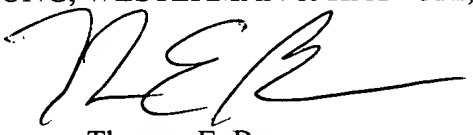
In view of the aforementioned amendments and accompanying remarks, claims 1 - 22, as amended, are in condition for examination, which action, at an early date, is requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. The attached page is captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE**".

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted

ARMSTRONG, WESTERMAN & HATTORI, LLP



Thomas E. Brown
Attorney for Applicant
Reg. No. 44,450

TEB/kal
Atty. Docket No. **990535**
Suite 1000, 1725 K Street, N.W.
Washington, D.C. 20006
(202) 659-2930

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PATENT TRADEMARK OFFICE

Enclosures: Version With Markings to Show Changes Made
Appended sheets of drawings (FIG. 2B, FIG. 4A and FIG. 4A-I)

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

Claims1, 9, 14, 16 and 21 have been amended as follows:

1. (Four Times Amended) A method of manufacturing a semiconductor device comprising the steps of :

forming a couple of impurity diffusion layers in a semiconductor substrate;

forming a first insulating film covering the semiconductor substrate;

forming a lower electrode of a capacitor on the first insulating film;

forming an oxide dielectric film of the capacitor on the lower electrode;

forming an upper electrode of the capacitor on the oxide dielectric film;

forming a second insulating film for covering the capacitor;

forming a first opening for electrically connecting one of the couple of impurity diffusion layers and a second opening which exposes the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film;

forming a metal film on the second insulating film for electrically connecting the one of the couple of impurity diffusion layers via the first opening and the upper electrode via the second opening, the metal film made of a member of the group consisting of a titanium nitride, a tungsten nitride, and titanium tungsten nitride;

forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view, the entire portion being with respect to a width and a length of the upper electrode, in a range which passes through the first opening and the second opening, by patterning the metal film;

forming a third insulating film for covering the local interconnection;

forming a third opening for electrically connecting to the other of the couple of impurity diffusion layers, by etching a part of the third insulating film; and

forming a wiring electrically connecting to the other of the couple of impurity diffusion layers, the wiring composed from [different material from the local interconnection] multi-layer films, the wiring having lower resistance than the local interconnection.

fig 23

page 15, line 23-26 not shown in the drawings
17, line 4-10

9. (Amended) A method of manufacturing a semiconductor device according to claim 1, wherein the oxide dielectric film is oxygen-annealed before [and/or] or after the upper electrode of the capacitor is formed.

14. (Three Times Amended) A method of manufacturing a semiconductor device according to claim 1 further comprising the step of:

forming a conductive plug between the metal film and [the] one of the couple of impurity diffusion layers in the first opening.

16. (Amended) A method of manufacturing a semiconductor device according to claim 1, wherein [the] one of the couple of impurity diffusion layers is a component part of an MOS transistor.

21. (Four Times Amended) A method of manufacturing a semiconductor device comprising the steps of :

forming a couple of impurity diffusion layers in a semiconductor substrate;

forming a first insulating film covering the semiconductor substrate;

forming a lower electrode of a capacitor on the first insulating film;

forming an oxide dielectric film of the capacitor on the lower electrode;

forming an upper electrode of the capacitor on the oxide dielectric film;

forming a second insulating film for covering the capacitor;

forming a first opening for electrically connecting one of the couple of impurity diffusion layers and a second opening which exposes the upper electrode in the first and second insulating films, by etching a part of the second insulating film and a part of the first insulating film;

forming a metal film on the second insulating film for electrically connecting the one of the couple of impurity diffusion layers via the first opening and the upper electrode via the second opening, the metal film made of a member of the group consisting of a titanium nitride, a tungsten nitride, and titanium tungsten nitride;

forming a local interconnection covering an entire portion of the upper electrode with an area which is larger than an area where the upper electrode contacts with the oxide dielectric film in a plan view, the entire portion being with respect to a width and a length of the upper electrode, in a range which passes through the first opening and the second opening, by patterning the metal film, wherein the local interconnection is a blocking layer for preventing a diffusion of a redundant to the oxide dielectric film;

forming a third insulating film for covering the local interconnection;

forming a third opening for electrically connecting to the other of the couple of impurity diffusion layers, by etching a part of the third insulating film; and

forming a wiring electrically connecting to the other of the couple of impurity diffusion layers, the wiring composed from [different material form the local interconnection] multi-layer films, the wiring having lower resistance than the local interconnection.